KEKON

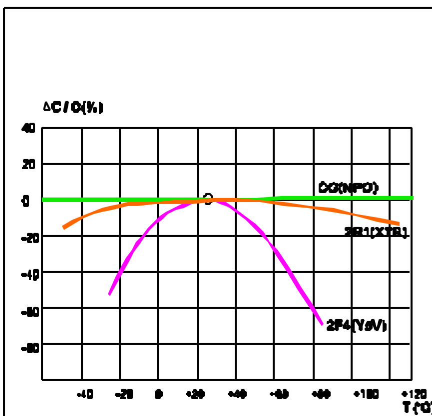
TECHNICAL DATA

PARAMETER	DIELECTRIC		
	CG (NP0)	2R1 (X7R)	2F4 (Y5V)
Measuring Frequency (for C, tanδ)	1 MHz for C≤1000pF 1 kHz for C>1000pF	1 MHz for C≤100pF 1 kHz for C>100pF	1 kHz
Capacitance Tolerance *	C, D, G ,J, K, M,	K, M, S, Z	M, S, Z
Dissipation Factor tanδ	15 10^{-4} for C≥50pF or 1.5(150/C+7)10^{-4}	350 10^{-4}	350 10^{-4}
Measuring Voltage (C, tanδ)	1 Vrms	0,3 Vrms	0,3 Vrms
Rated Voltage	16V – 10kV		
Test Voltage (16V – 10kV) **	16 - 100V 2,5xUr 200 – 500V 1,5xUr + 100V > 500V 1,2xUr		
Insulating Resistance Ri	≥10GΩ or RixC≥100ΩF whichever is less	≥4GΩ or RixC≥100ΩF whichever is less	≥4GΩ or RixC≥100ΩF whichever is less
Measuring Voltage (for Ri)	16-500V Ur >500V 500V		
Temperature Range	-55°C to +125°C	-55°C to +125°C	-25°C to +85°C
Temperature Characteristics	0 ± 30 ppm/°C	± 15%	+30% / -80%
Climatic Category	55 / 125 / 56	55 / 125 /56	25 / 85 / 21
Reference Temperature	23^0C		
Voltage Dependence	No	Yes	Yes
Aging (per hour decade)	0	<2%	<6%
Termination (chip)	AgPd or Ni barrier or Cu/Sn		
Packaging	Bulk or Taped		
Standard	IEC 384 – 10 IEC 384 –8,9 for leaded IEC 60286-3 for taped SMD		

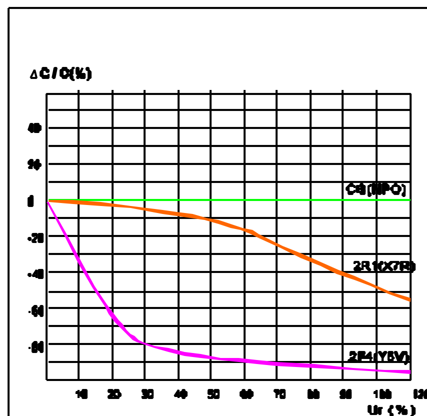
* *Capacitance tolerance, see Ordering Code*

** *Units rated above 1000V may require conformal coating in use to preclude arcing over the chip surface*

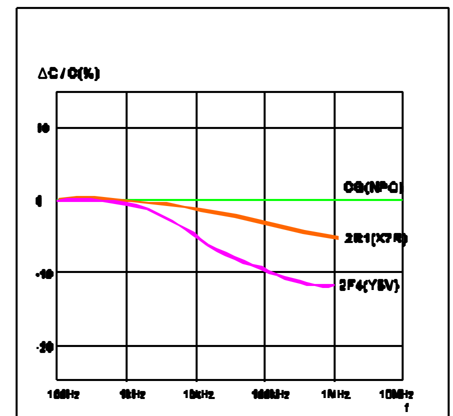
Capacitance as a function of temperature



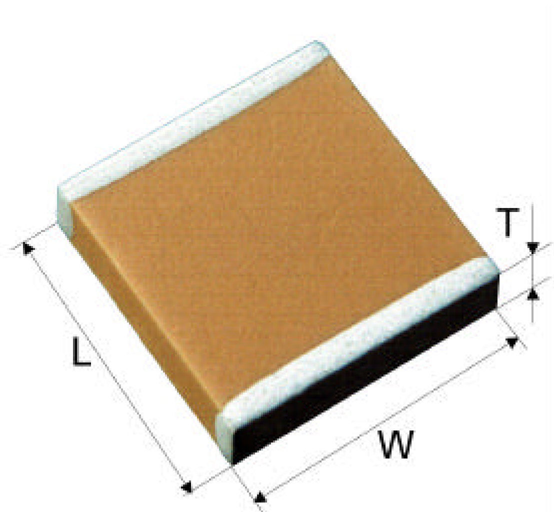
Capacitance as a function of DC voltage (Ur=50V)



Capacitance as a function of frequency



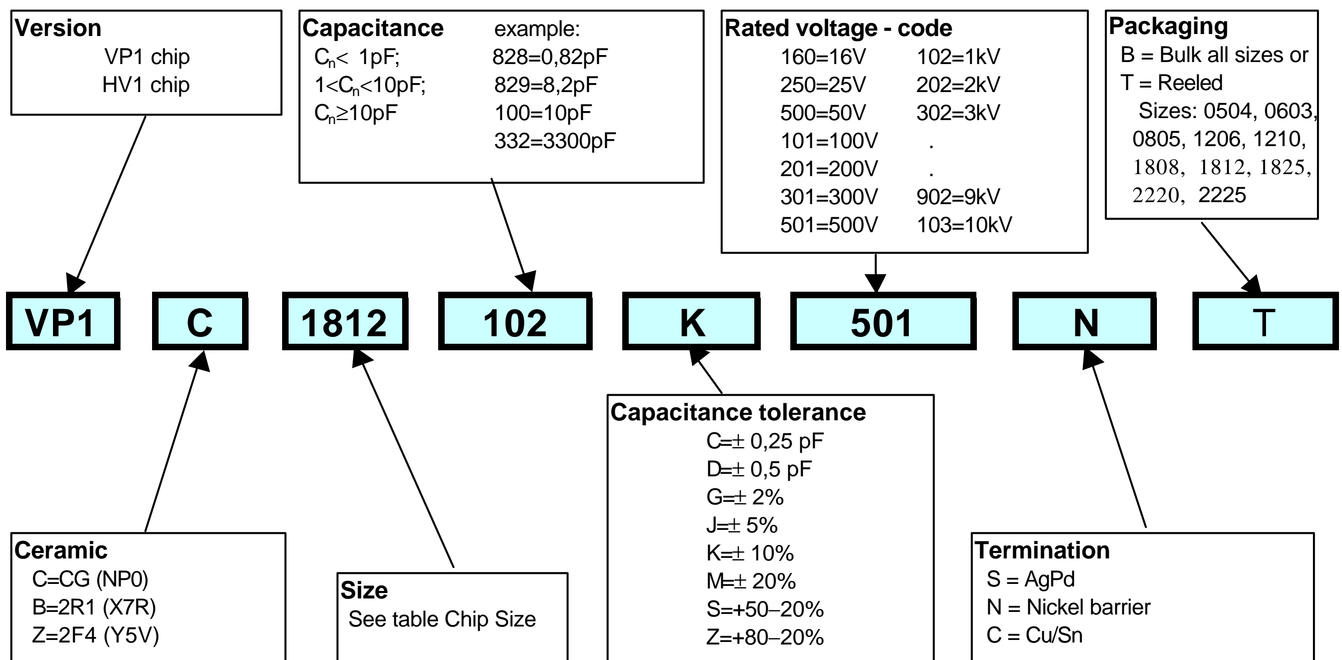
CHIP SIZE 16 – 10000 Vdc



Size	L	W	T_{max}
0504	1.25 $^{\pm0.15}$	1.0 $^{\pm0.1}$	0.95
0603	1.6 $^{\pm0.15}$	0.8 $^{\pm0.15}$	0.95
0805	2.0 $^{\pm0.2}$	1.25 $^{\pm0.2}$	1.2 *
1206	3.2 $^{\pm0.3}$	1.6 $^{\pm0.2}$	1.5 *
1210	3.2 $^{\pm0.4}$	2.5 $^{\pm0.3}$	2,5
1808	4.5 $^{\pm0.4}$	2.0 $^{\pm0.3}$	2,0
1812	4.5 $^{\pm0.5}$	3.2 $^{\pm0.4}$	3.0
1825	4.5 $^{\pm0.5}$	6.3 $^{\pm0.5}$	3.0
2220	5.7 $^{\pm0.5}$	5.0 $^{\pm0.5}$	3.0
2225	5.7 $^{\pm0.5}$	6.3 $^{\pm0.5}$	3.0
1515	3.8 $^{\pm0.4}$	3.8 $^{\pm0.4}$	3.0
2020	5.0 $^{\pm0.5}$	5.0 $^{\pm0.5}$	4.0
2520	6.3 $^{\pm0.5}$	5.0 $^{\pm0.5}$	4.0
3530	8.89 $^{\pm0.9}$	7.62 $^{\pm0.8}$	5.0
4020	10.2 $^{\pm0.1}$	5.0 $^{\pm0.5}$	5.0
4040	10.2 $^{\pm0.1}$	10.2 $^{\pm0.1}$	5.0
4540	11.4 $^{\pm0.1}$	10.2 $^{\pm0.1}$	5.0
5040	12.7 $^{\pm0.2}$	10.2 $^{\pm0.1}$	6.5
5440	13.7 $^{\pm0.14}$	10.2 $^{\pm0.1}$	6.5
5550	14.0 $^{\pm0.14}$	12.7 $^{\pm0.13}$	6.5
6560	16.5 $^{\pm0.16}$	15.2 $^{\pm0.15}$	6.5
6660	16.7 $^{\pm0.16}$	15.2 $^{\pm0.15}$	6.5
7565	19.50 $^{\pm0.19}$	16.5 $^{\pm0.16}$	6.5

Tmax 0,63mm available on request

Ordering Code



RECOMMENDATION FOR SURFACE MOUNTING

1. Soldering Methods:
Soldering methods commonly used in the industry and recommended are Infrared Reflow Soldering, Wave Soldering and Vapor Phase Soldering. If hand soldering cannot be avoided care should be taken not only in soldering, but also in correct component handling.

2. Solder Heat and Thermal Shock:
Ceramic material is very sensitive to quick changes in temperature, therefore it is very important to avoid sudden temperature cycles during the soldering process. Sudden heating may cause microcracks in the ceramics and consequently may reduce the insulation resistance and withstand voltage. The risk increases with the size of the chips.

All soldering methods involve thermal cycling of the capacitors. The rate of heating and cooling must be controlled to avoid thermal shocks cracking of the MLC chips. In general the components should be preheated with a heating speed of around 2°C per second and even slower for large chips, up to a temperature of maximum 100°C under soldering temperature (ΔT). A soak at the end of the pre-heat is useful when larger components are soldered.
A recommended Temperature - Time profile for most soldering systems is shown in Fig. 1

3. Solder Time:
Solder melting time should be minimized. The maximum permissible solder time that a MLC chip may be subjected to is depended upon the termination material and soldering process and temperature of solder.
Figure 2 shows comparative Temperature / Time data for silver palladium and nickel barrier or tinned copper terminations.

Typical solder times are:

Wave Soldering	3 - 5 sec.at 250°C
Infrared Reflow	7 - 10 sec. at 225°C
Vapor Phase	15 - 20 sec. at 215°C

Cooling to ambient should be allowed to occur naturally.

4. Handling:
Chip ceramic capacitors should be handled with care to avoid any mechanical damage and chip surface contamination.

5. Solderability:
Applying a midlly activated fluxes are preferred. Terminations should be well soldered after immersion in a solder bath (60Sn/40Pb) at 235±5°C for 2±1sec.

6. Solder Deposition
If too much solder is deposited, the chip will become more susceptible to the thermal and mechanical stress that result from solder contraction, and it could break. If not enough solder is deposited, adhesion to the terminal electrodes will be weak, which could the chip to work loose. A solder film thickness of 200 – 250 µm is recommended.

7. Cleaning:
MLC chip capacitors can withstand the commonly used cleaning agents, such as water, alcohol and degreaser solvents. Be careful that no flux residues are left on the chip surface.

8. Shelf Life:
Capacitors will be solderable for a minimum of one year from the date of shipment, if they are stored properly (dry environment) in the original packaging.

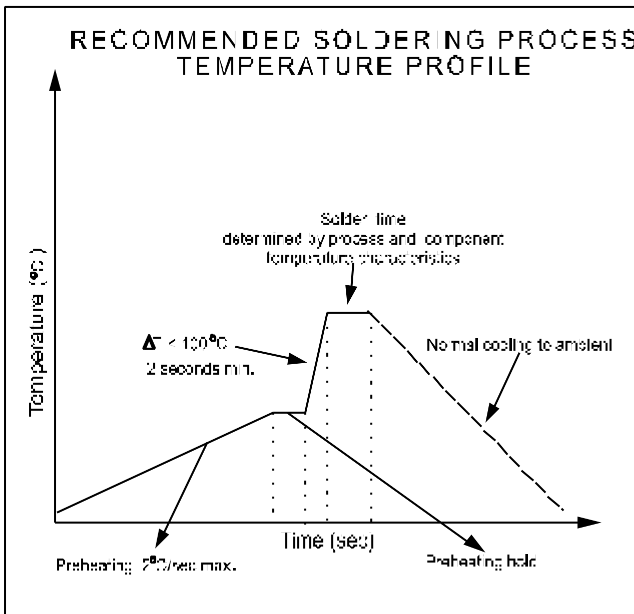


Fig. 1: Recommended Soldering Process Profile

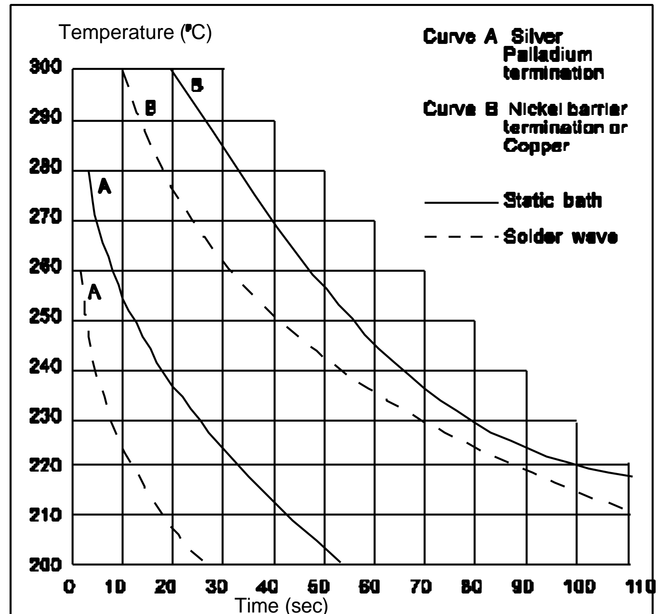
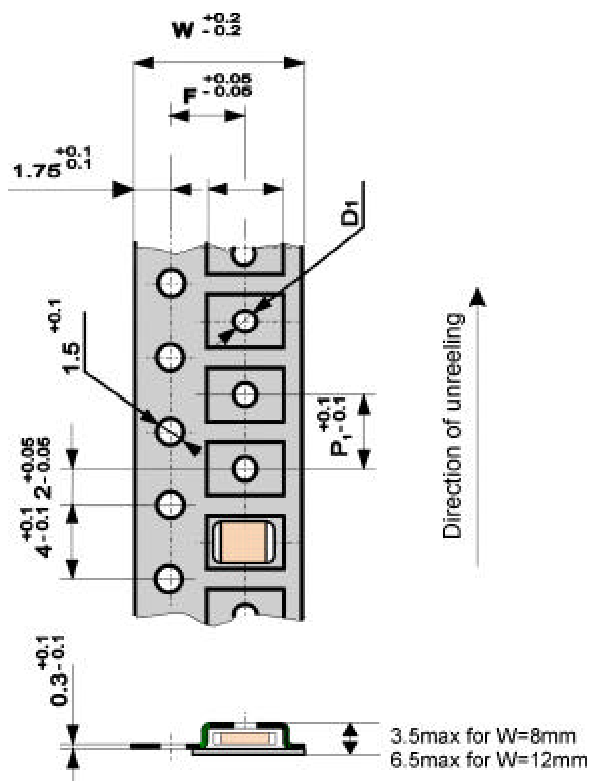


Fig. 2: Solder Time Temperature Curves

PACKAGING



Tape dimensions

(Unit: mm)

Size	0504	0603	0805	1206	1210	1808	1812	1825	2220	2225
P_1	4	4	4	4	4	8	8	8	8	8
F	3.5	3.5	3.5	3.5	3.5	5.5	5.5	5.5	5.5	5.5
W	8	8	8	8	8	12	12	12	12	12
T	8.4	8.4	8.4	8.4	8.4	12.4	12.4	12.4	12.4	12.4
D_1 min	1	1	1	1	1	1.5	1.5	1.5	1.5	1.5

Packing unit

(Unit max: pcs)

Size	0504	0603	0805	1206	1210	1808	1812	1825	2220	2225	1515
Reel 180mm	4.000	4.000	4.000	4.000	4.000	1.500	1.500	1.000	1.000	1.000	/
Reel 330mm	16.000	16.000	16.000	16.000	16.000	6.000	6.000	4.000	4.000	4.000	/
Bulk 200x100x50mm	12.000	12.000	12.000	12.000	12.000	3.000	3.000	3.000	3.000	3.000	3000

Size	2020	2520	3530	4020	4040	4540	5040	5440	5555, 6560, 6560, 7565
Bulk 200x100x50mm	3.000	3.000	2.000	2.000	1.000	1.000	1.000	1.000	500

Quantity per reel varies with the chip thickness.